REMARKS

Claim Rejections Under 35 USC §103

Claims 24-36 have been rejected under 35 USC 103(a) as being unpatentable over the admitted prior art (APA) in view of Lee et al. (U.S. Patent No. 5,796,586) and/or Akram et al. (US Patent No. 5,739,585).

Claims 27-29 have been rejected under 35 USC 103(a) as being unpatentable over the admitted prior art (APA) in view of Lee et al. (U.S. Patent No. 5,796,586) and/or Akram et al. (US Patent No. 5,739,585).

Claims 30-33 have been rejected under 35 USC 103(a) as being unpatentable over the admitted prior art (APA) in view of Lee et al. (U.S. Patent No. 5,796,586) and/or Akram et al. (US Patent No. 5,739,585).

Claims 34-36 have been rejected under 35 USC 103(a) as being unpatentable over the admitted prior art (APA) in view of Lee et al. (U.S. Patent No. 5,796,586) and/or Akram et al. (US Patent No. 5,739,585).

The 35 USC §103 rejections are traversed for the reasons to follow.

Summary of the Invention

The claims are directed to a board-on-chip semiconductor package 62 (Figure 6B). As shown in Figure 6B, the BOC package 62 includes a substrate 56 comprising a first surface 44 with a pattern of conductors 48, an opposing second surface 46 with a die attach area 50, and a wire bonding opening 64 extending through the substrate 56 from the first surface 44 to the second surface 46. In addition, the package 62 includes a first solder mask 80A having openings 82 for attaching solder balls 88 to the conductors 48, and an opening 84 (Figure 3C) for wire bonding to the conductors 48. The package 62 also includes a second solder mask 80B having an opening 86 (Figure 3D) on the die attach area 50.

As also shown in Figure 6B, the package 62 includes a semiconductor die 16 placed face down (circuit side down) through the opening 86 in the second solder mask 80B, and attached directly to the substrate 56 in the die attach area 50. An adhesive layer 72 (Figure 6A) attaches the face of the die 16 directly to the substrate 56. The package 62 also includes wires 94 placed through the wire bonding opening 64 in the substrate 56, and bonded to bonding pads on the face of the die 16, and to bonding pads 52 (Figure 6A) on the conductors 48. In addition, solder balls 88 are placed through the openings 82 in the first solder mask 80A, and attached to ball bonding pads 54 (Figure 6A) on the conductors 48. As also shown in Figure 6B, an encapsulating resin 90 is molded over the die 16, and over the second solder mask 80B. Further, a glob top 92 can be placed over the wires 94, and in the wire bonding opening 64 to protect the wire bonds.

Argument

35 USC §103 Rejections Over Admitted Prior Art, Lee et al. and Akram et al.

Claims 26, 27, 30, 32, 33 and 36 have been amended to emphasize the feature of the face of the die being bonded directly to the substrate in the open die attach area using a "filled adhesive configured to transfer heat directly from the face to the substrate". Antecedent basis for the additional recitations is contained on page 11, lines 28-30 and on page 12, lines 9-10 of the specification.

This feature is not disclosed by the combination of the admitted prior art, Lee et al. and Akram et al. In addition, this feature, in combination with other features of the package, make claims 26-33 and 36 "taken as a whole" unobvious over the prior art. Further, MPEP 2142, 2143, which set forth the three basic criteria for establishing a prima facie case of obviousness under 35 USC §103(a), require

that a cited combination of references teach or suggest all the claim limitations.

The admitted prior art discloses a board-on-chip package 10 (Figure 1A) in which the die 16 is bonded face down to the solder mask 22, rather than directly to the substrate in an open die attach area as presently claimed. The solder mask 22 provides an impediment for heat transfer between the die 16 and the substrate.

Lee et al. is a chip on board package, rather than a board on chip package as presently claimed, such that the die 220 (Figure 6) is back bonded to the substrate 216. Most of the heat in a die is generated near the face where the integrated circuits are located. Thus in Lee et al. the semiconductor substrate of the die, and any coating on the back side of the die, provide an impediment to heat transfer to the substrate. Lee et al. discusses die attach adhesives at column 6, lines 32-36. However, filled adhesives which are configured to improve heat transfer are not mentioned in Lee et al. In addition, the concept of improved heat transfer is not suggested

Akram et al. teaches attaching a die 18 face down to a package body 12 using an adhesive layer (column 4, lines 25-29). In this regard the Office Action states at page 4, line 2 that Akram et al. teaches typical adhesive/fill materials. However, a filled adhesive layer is not mentioned in Akram et al., and the concept of improved heat transfer between the face of the die 18 and the package body 12 is not suggested.

A second feature recited in independent claims 24, 27 and 34 is also not taught or suggested by the cited combination of art. This is the feature of the opening in the second solder mask being only slightly larger than the outline of the die. For example, claim 24 recites "a second outline corresponding to but only slightly larger than the first outline". The encapsulating resin 90 attaches directly to the second solder mask 80A and the die 16 rather than to the substrate 56. Improved adhesion between the

encapsulating resin 90 and the substrate 56 is provided. In Lee et al. the opening in the solder mask and the die attach area 204 (Figure &) must be large enough to accommodate wire bonding of the die. The encapsulating resin therefore is formed on a large area of the substrate which may not provide as good adhesion as the solder mask.

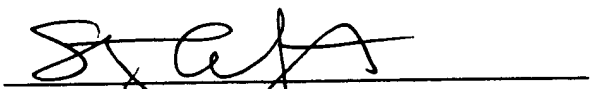
The Office Action characterizes this feature as a "design choice ... to achieve the desired bonding with the encapsulant and adhesion". However, Lee et al. does not recognize that making the surface area of the solder mask as large as possible also improves the adhesion. This is despite the fact that a primary object in Lee et al. is to improve the adhesion of the encapsulant using the anti adhesive solder mask. In view of the significance of this improvement, Applicant would characterize this feature as more than a mere design choice. Independent claim 27 recites this feature in combination with the above argued "filled adhesive" and "direct heat transfer" feature.

Conclusion

In view of the above arguments and amendments, favorable consideration and allowance of claims 24-36 is respectfully requested. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

DATED this 13th day of March, 2002.

Respectfully submitted:



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Marked Version Of Amended Claims Showing Changes

26. (four times amended) The package of claim 25 wherein the adhesive layer comprises a filled adhesive configured to transfer heat directly from the face to the second surface.

27. (four times amended) A semiconductor package comprising:

a substrate comprising a first surface, a second surface, a plurality of conductors on the first surface comprising ball bonding pads and wire bonding pads, and a bonding opening from the first surface to the second surface;

a semiconductor die having a first outline, the die comprising a face on the bonding opening bonded to the second surface;

a first mask on the first surface comprising a plurality of via openings aligned with the ball bonding pads and a first opening exposing the wire bonding pads;

a second mask substantially covering the second surface comprising a second opening having a second outline corresponding to but only slightly larger than the first outline to define an open die attach area on the second surface;

[an] a filled adhesive layer between the die and the substrate in the open die attach area bonding the face to the second surface and transferring heat directly from the face to the substrate;

a plurality of wires in the bonding opening wire bonded to the die and to the wire bonding pads; and

an encapsulating resin on the die and on the second mask.

30. (five times amended) A semiconductor package comprising:

a substrate having a first surface, a second surface and a bonding opening there through;

a plurality of conductors on the first surface; [comprising a plurality of ball bonding pads;]

a first mask on the first surface at least partially covering the conductors;

[comprising a plurality of via openings to the ball bonding pads;]

[a semiconductor die having a face on the bonding opening attached directly to the second surface;]

a second mask covering the second surface except in a die attach area defined by an opening through the second mask;

[having an outline corresponding to but only slightly larger than that of the face;]

a semiconductor die on the die attach area having a face aligned with the bonding opening and attached to the second surface;

a filled adhesive layer attaching the die to the substrate in the open die attach area configured to transfer heat directly from the face to the second surface;

[a plurality of solder balls in the via openings bonded to the ball bonding pads;]

a plurality of wires placed through the bonding opening and bonded to the die and to the conductors; and

an encapsulating resin on the second mask encapsulating the die.

32. (four times amended) The package of claim 30 further comprising a polymer in the bonding opening and on the first surface at least partially encapsulating the wires.

[plurality of wire bonding pads on the conductors wire bonded to the wires and a second opening in the first mask exposing the wire bonding pads.]

33. (four times amended) The package of claim 30 [further comprising a filled] wherein the adhesive layer comprises a filled epoxy.
[attaching the die to the substrate in the open die attach area.]

36. (four times amended) The package of claim 34 wherein the adhesive layer comprises a filled epoxy configured to transfer heat directly from the face to the substrate.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner of Patents, BOX RCE, Washington, D.C. 20231 on this 13th day of March, 2002.

March 13, 2002
Date of Signature

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